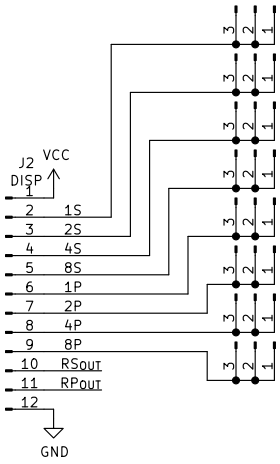
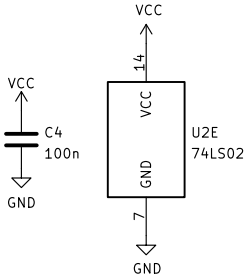
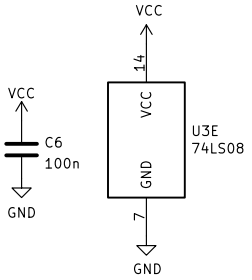
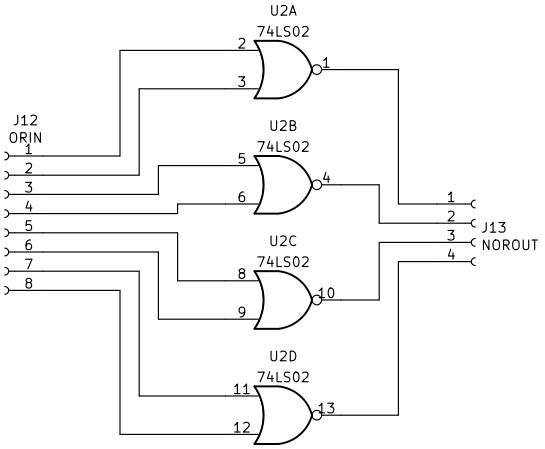


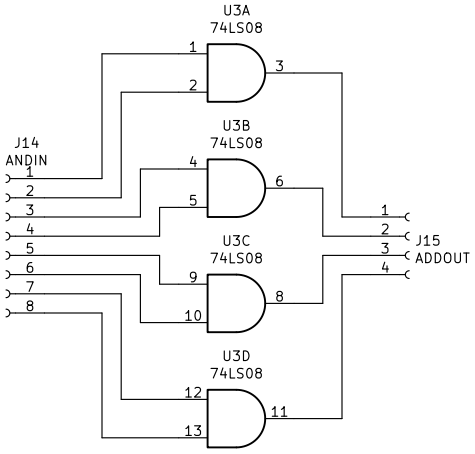
Connector to Display

All the signals (and power) is exchanged via this connector to the display boards









Logic Gates

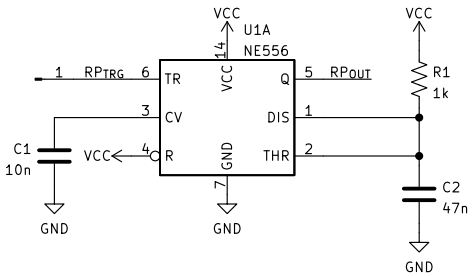
The signals between logic gates and the the main connector must be done by hand by the user using jumper wires between the pads for each respective signal.

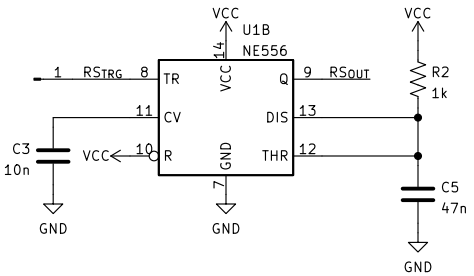
NOTE: TWO SEPERATE SIGNALS SHOULD NEVER BE SHORTED TOGETHER TO AVOID DAMAGE IF THEY TRY TO DRIVE THE SHARED CONNECTION DIFFERENT WAYS!

Reset Pulse Timers

Since there were issues stemming from the short and noisy reset pulses produced by logic chips directly (since the feedback to end the pulse was too quick). Additional circuitry is used to issue a set length reset pulse once triggered using 555 timers in mono-stable mode (output when triggered).

NOTE: TRIGGER USES NEGATIVE LOGIC ("HIGH" FOR "OFF")





Pulses are roughly 50 microseconds long, but anything longer than 1 microsecond should be fine.

556 timer used to ensure consistent reset pulses
User configured logic for resetting counters
Configured using wires soldered between headers

Title: Clock Reset Logic		
Savo Bajic	Date: 2022-03-27	**Rev: 2**
KiCad E.D.A. kicad 6.0.1-79c1e3a40b-116-ubuntu21.04.1	Size: USLetter	Sheet: 1/1